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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/758,863	01/16/2004	Robert B. Staszewski	TI-35773	6568

23494 7590 09/11/2009

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EXAMINER	
FLORES, LEON	

ART UNIT	PAPER NUMBER
2611	

NOTIFICATION DATE	DELIVERY MODE
09/11/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/758,863	STASZEWSKI ET AL.	
	Examiner	Art Unit	
	LEON FLORES	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 June 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-54* is/are pending in the application.

4a) Of the above claim(s) *4* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 5-54* is/are rejected.

7)☒ Claim(s) *12, 18, 26* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

In view of the appeal brief filed on 6/16/2009, PROSECUTION IS HEREBY REOPENED. An Ex-Parte Quayle (or new ground of rejection) set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) initiate a new appeal by filing a notice of appeal under 37 CFR 41.31 followed by an appeal brief under 37 CFR 41.37. The previously paid notice of appeal fee and appeal brief fee can be applied to the new appeal. If, however, the appeal fees set forth in 37 CFR 41.20 have been increased since they were previously paid, then appellant must pay the difference between the increased fees and the amount previously paid.

A Supervisory Patent Examiner (SPE) has approved of reopening prosecution by signing below:

Response to Arguments

1. Applicant's arguments with respect to claims (1-54) have been considered but are moot in view of the new ground(s) of rejection.

Applicant asserts that *"Staszewski teaches an all-digital phase-locked loop (ADPLL), which contains a digital phase error (PHE) signal. The reference describes an apparatus but does not teach or even suggest a method of testing it".*

The examiner agrees. However, a new ground of rejection has been issued.

Applicant further asserts that *"Examiner's new determination that, "one skilled in the art would know that by filtering out frequencies components (not desired) which are above the cut off frequency of the loop filter, a high degree of correlation between the phase error (desired frequencies) and the RF output can be achieved - this is notoriously well known in ADPLLs (OA, page 3, lines 12-16)". Examiner's determination is not correct. While PLL filtering of external signals is well known, use of PLL filtering for "internal" signals, as required by the limitation "signal from within a processing portion of the RF circuit", is not known. In the event Examiner does not withdraw this determination, Appellants requested that Examiner cite a reference to support this determination - but Examiner refused".*

The examiner respectfully disagrees. One skilled in the art would know that, by definition, a loop filter filters out high frequency components that are not of interest, and passes only low frequency components that are of main interest to the PLL. (See pages 604-605 of "Digital Communications" by Bernard Sklar) Furthermore, applicant does teach in his specifications that "As long as the frequency components of interest are below the loop filter's cutoff frequency, the attenuation of frequency components above the cutoff frequency can actually improve the correlation between the observed signal and the RF output".

Applicant further asserts that *"Examiner's contention that one skilled in the art "would know that if the loop filter is designed in such as way (adjusting filter's parameters) so that the frequency of the error signal is within the cutoff frequency of the*

loop filter, then a high degree of correlation can be achieved between the error signal and the output signal". Appellants respectfully request Examiner to provide evidence from the prior art supporting his assertion or withdraw the determination. Furthermol~e, when a high degree of correlation is achieved the transfer function will be flat within a specific frequency range". At the time of the instant application, thc knowledge that the digital PHE signal was highly correlated with the RF output phase, and their transfer function was fiat, was not obvious".

The examiner respectfully disagrees. One skilled in the art would know that, by definition, a loop filter filters out high frequency components that are not of interest, and passes only low frequency components that are of main interest to the PLL. (See pages 604-605 of "Digital Communications" by Bernard Sklar) Furthermore, applicant does teach in his specifications that "As long as the frequency components of interest are below the loop filter's cutoff frequency, the attenuation of frequency components above the cutoff frequency can actually improve the correlation between the observed signal and the RF output".

Now, if there some kind of correlation between the phase error and the RF output, then its transfer function (RF output divided by the phase error) would be flat at certain frequency range since there is a high degree of correlation.

Applicant further asserts that *""loop type" is not a proper way of "setting the all-digital phase-locked loop to a certain bandwidth". Changing of loop type only introduces a pole at origin and does not control its bandwidth. At best, its effect would be parasitic*

or useless for a practical application. For the reasons set forth above, any combination of Staszewski and Wong fails to teach or suggest all of the elements of Claim 24. The 35 U.S.C. 103(a) rejection is erroneous and must be withdrawn".

The examiner respectfully disagrees. Applicant's assertion that "changing of loop type only introduces a pole at origin and does not control its bandwidth" is erroneous. Each of these loop type introduces a number of different types of zeroes and poles. One skilled in the art would know that the bandwidth is dependent on the number of zeros and poles and its arrangement.

Applicant further asserts that *"In contrast, Wong describes a phase locked loop (PLL) nominally operating at 125 MHz for clock recovery of a 125 Mbits/s FDDI data. The PLL contains access ports connected to an I/O controller that interfaces with an external Tester 4. The PLL consists of a Phase Detector 10, Phase Error Processor (PEP) 12 performing phase error decimation and quantization and outputting 1-bit digital signal carrying UP/DOWN and Data_valid flag, Loop Filter 14 controlled by Loop Configuration Port (LCP) 24, Phase-to-Frequency Converter (PFC) 16 to generate a triangular wave of controllable frequency, and a Frequency Controlled Oscillator (FCO) 18. The FCO operates at two times the output frequency and is fed by equally-spaced 250 MHz clock and is followed by a divide-by-two 20 circuit. The loop filter integral signal couples with Frequency Access Port (FAP) 26. The accumulated ("sawtooth patterns") up/down bits are coupled with the Phase Access Port (PAP) 28. The PEP outputs arc decimated by 44, so its output data rate as well as any other 'down-stream'*

circuit until the FCO is 125Mbps/44=2.84Mbps. The I/O controller link 6 connects the tester 4 with the LCP 24, FAP 26 and PAP 28. Wong's system is engineered in such as way as to minimize the data rate accessible through the I/O controller. Hence, the phase detector 10 output is not accessible nor is the PEP 12 output - making them available (despite various technical difficulties) would not provide any substantial benefits. For the above reasons, Wong does not teach or suggest, "a control signal input coupled to the processor, wherein the control signal input can enable an observation and manipulation of the digital signals." The interface in Wong is asynchronous and there is simply no motivation to re-engineer the entire architecture, which in itself is non-obvious to one of average skill in the art at the time of the invention, to allow synchronous signal controls of sufficient speed, as suggested by Examiner".

The examiner respectfully disagrees. Applicant is reminded that **MPEP 2141.02** states:

A prior art reference must be considered in its entirety, i.e., as a whole, including portions that would lead away from the claimed invention. W.L. Gore & Associates, Inc. v. Garlock, Inc., 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983), cert. denied, 469 U.S. 851 (1984)

Having said this, applicant is silent with regards to col. 3, lines 50-55 wherein Wong explicitly teaches that "the output of the digital integrator of the DPLL loop filter reflect the frequency difference between the local clock and the incoming data to the DPLL.

The integral signal content is accessible via the FAP 26 through which the digital tester can either read the error frequency". One skilled in the art would know that frequency and phase are related to one another. Therefore, the reference of Wong does teach a digital tester capable of accessing and manipulating the digital signals, as claimed.

Applicant further asserts that *"Moreover, Wong does not teach or suggest the limitation of "to provide a performance metric for the RF circuit", as further required by Claim 32. Wong teaches only testing and does not even suggest performance estimation. Accordingly, the 35 U.S.C. 103(a) rejection is improper and must be withdrawn".*

The examiner respectfully disagrees. Applicant is reminded that **MPEP 2141.02** states:

A prior art reference must be considered in its entirety, i.e., as a whole, including portions that would lead away from the claimed invention. W.L. Gore & Associates, Inc. v. Garlock, Inc., 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983), cert. denied, 469 U.S. 851 (1984)

The reference of Wong does explicitly teach "providing a performance metric for the RF circuit". (See col. 1, lines 42-61)

Applicant further asserts that *"It does not teach performance testing associated with a cellular phone, nor does it even go beyond the PLL, which is merely a small*

building block of a cell phone. Specifically he does not teach "performing built-in self-test (BIST) on a parameter associated with the cellular phone", as required by Claim 48".

The examiner respectfully disagrees. First of all, it is notoriously well known in the art that cellular phones are comprised of many electrical components. And one of these components is the PLL. Second of all, the reference of Kim does teach performing BIST on a PLL in order to determine its performance. (See col. 3, lines 9-21) And finally, applicant is reminded that **MPEP 2141.02** states:

A prior art reference must be considered in its entirety, i.e., as a whole, including portions that would lead away from the claimed invention. W.L. Gore & Associates, Inc. v. Garlock, Inc., 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983), cert. denied, 469 U.S. 851 (1984)

Applicant finally asserts that *"At best, Perez teaches basic fault testing, but NOT "built-in self-test (BIST) on a parameter associated with the cellular phone", as required by Claim 48. Accordingly, for the reasons set forth above, the 35 U.S.C. 103(a) rejection of Claim 48 is improper and must be withdrawn".*

The examiner respectfully disagrees. First of all, applicant is reminded that **MPEP 2141.02** states:

A prior art reference must be considered in its entirety, i.e., as a whole, including portions that would lead away from the claimed invention. W.L. Gore & Associates, Inc.

v. Garlock, Inc., 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983), cert. denied, 469 U.S. 851 (1984)

Having said this, the reference of Perez does teach the concept of using a self-diagnostic system for checking all functions of a cellular-transceiver system and reporting the results to an off-site monitoring center. (See col. 3, lines 50-67)

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. The factual inquiries set forth in *Graham* **v.** *John Deere Co.,* 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. **Claims (1-3, 5-11, 13-17, 19-23, 25, 27-31) are rejected under 35 U.S.C. 103(a) as being unpatentable over Sunter et al. (hereinafter Sunter) (US Patent 6,396,889 B1)**

Re claim 1, Sunter discloses a method for testing a radio frequency (RF) circuit comprising: observing a signal from the RF circuit (See figs. 5, 9 & 11 "the error signal is

observed using test circuits" See col. 2, lines 50-54, col. 3, lines 4-6 & fig. 9 & col. 8, lines 9-16), wherein the signal is a digital signal from within a processing portion of the RF circuit (See fig. 5 "Exor Output is a digital signal"), and wherein the observing occurs outside of the RF circuit (See figs. 5, 9 & 11"the observation is done using test circuits such as BIST"); manipulating (See fig. 11 & col. 3, lines 4-6) the signal outside of the RF circuit ("a test circuit is used to test phase jitter"); and producing a metric for the test outside of the RF circuit based on results from the manipulating. (phase jitter is compared to a metric to determined a Pass or Fail")

But the reference Sunter fails to explicitly teach that wherein the signal has a high degree of correlation with an RF output of the RF circuit.

However, the reference of Sunter does teach a PLL having a loop filter connected at the output of the phase comparator whereby suggesting that wherein the signal has a high degree of correlation with an RF output of the RF circuit. (See figs. 5 & 9) One skilled in the art would know that, by definition, a loop filter filters out high frequency components that are not of interest, and passes only low frequency components that are of main interest to the PLL. (See pages 604-605 of "Digital Communications" by Bernard Sklar) Furthermore, applicant does teach in his specifications that "As long as the frequency components of interest are below the loop filter's cutoff frequency, the attenuation of frequency components above the cutoff frequency can actually improve the correlation between the observed signal and the RF output".

Therefore, it would have been obvious to one of ordinary skills in the art to incorporate this feature into the system of Sunter, in the manner as claimed, for the benefit of filtering out frequency components that are not of interest.

Re claim 2, Sunter further discloses that wherein the testing is performed using built-in self test (BIST) techniques. (See col. 4, lines 10-15)

Re claim 3, Sunter further discloses that wherein the signal is a phase error signal. (See figs. 5 & 11)

Re claim 5, the reference Sunter fails to explicitly teach that wherein a transfer function between the signal and the RF output phase is flat within a frequency band of interest.

However, the reference of Sunter does teach a PLL having a loop filter connected at the output of the phase comparator whereby suggesting that wherein the signal has a high degree of correlation with an RF output of the RF circuit, and that wherein a transfer function between the signal and the RF output phase is flat within a frequency band of interest. (See figs. 5 & 9) One skilled in the art would know that, by definition, a loop filter filters out high frequency components that are not of interest, and passes only low frequency components that are of main interest to the PLL. (See pages 604-605 of "Digital Communications" by Bernard Sklar) Furthermore, applicant does teach in his specifications that "As long as the frequency components of interest

are below the loop filter's cutoff frequency, the attenuation of frequency components above the cutoff frequency can actually improve the correlation between the observed signal and the RF output".

Therefore, it would have been obvious to one of ordinary skills in the art to incorporate this feature into the system of Sunter, in the manner as claimed, for the benefit of filtering out frequency components that are not of interest.

Re claim 6, Sunter further discloses that wherein the RF circuit is an all-digital circuit, and wherein the signal is an output of a component in an all-digital phase-locked loop in the RF circuit. (See fig. 5)

Re claim 7, Sunter further discloses that wherein the signal is an output of a phase detector. (See fig. 5)

Re claim 8, Sunter further discloses that wherein the signal has been filtered. (See fig. 5)

Re claim 9, Sunter further discloses that wherein the all-digital phase-lock loop is operating in a type-II mode, and the signal is an output of an integral accumulator of a loop filter. (See fig. 3: 20)

Re claim 10, Sunter further discloses that wherein the all-digital phase-lock loop is operating in a type-I mode, and the signal is an output of an infinite impulse response filter coupled to the output of a loop filter. (See fig. 5: 28)

Re claim 11, Sunter further discloses that wherein a loop filter coupled to an output of a phase detector performs the filtering, and wherein the signal is an output of the loop filter. (See figs. 3 & 5)

Re claim 13, Sunter further discloses that wherein the frequency of the signal is several orders of magnitude less than the frequency of the RF output. (One skilled in the art would know that the frequency of the error signal, outputted from the phase comparator, is less than the RF frequency.)

Re claim 14, Sunter further discloses that wherein the test is for phase error trajectory and the signal is the output of a phase detector, and wherein the manipulation comprises measuring a change in the signal. (See col. 8, lines 9-37)

Re claim 15, Sunter further discloses that wherein the phase error trajectory is good when the change in the signal is less than a specified threshold. (See col. 9, lines 54-65)

Re claim 16, Sunter further discloses that wherein the measuring the change in the signal comprises measuring a peak, a variance, or a rate of change in the signal. (See col. 9, lines 54-65)

Re claim 17, Sunter further discloses that wherein the test is for frequency lock and the signal is the output of a phase.detector, and wherein the manipulation comprises comparing a value of the signal over several samples. (See fig. 8 "frequency locked")

Re claim 19, Sunter further discloses that wherein the samples are taken at different times. (See fig. 8 "Lock range")

Re claim 20, Sunter further discloses that wherein the test is for frequency deviation and the signal is an output of an integral accumulator of a loop filter, and wherein the manipulation comprises comparing the signal with a specified range. (See fig. 8 "Lock range")

Re claim 21, Sunter further discloses that wherein the frequency deviation is within acceptable limits when the signal is within the specified range. (See fig. 8 "Lock range")

Re claim 22, Sunter further discloses that wherein the manipulation further comprises comparing several samples of the signal. (See fig. 8 "Lock range")

Re claim 23, Sunter further discloses that wherein the RF circuit contains an all-digital phase-locked loop operating in a type-II mode. (See fig. 3: 20)

Re claim 25, Sunter discloses a method for testing a radio frequency (RF) circuit comprising: observing a signal from the RF circuit (See figs. 5, 9 & 11 "the error signal is observed using test circuits" See col. 2, lines 50-54, col. 3, lines 4-6 & fig. 9 & col. 8, lines 9-16), wherein the signal is a digital signal from within a processing portion of the RF circuit (See fig. 5 "Exor Output is a digital signal"), and wherein the observing occurs outside of the RF circuit (See figs. 5, 9 & 11. "the observation is done using test circuits such as BIST"); manipulating (See fig. 11 & col. 3, lines 4-6) the signal outside of the RF circuit ("a test circuit is used to test phase jitter"); and producing a metric for the test outside of the RF circuit based on results from the manipulating (Phase jitter is compared to a metric to determined a Pass or Fail"), and wherein the test is for estimating phase noise power and the signal is an output of a phase detector ("phase jitter is a function of phase noise"), and wherein the manipulating comprises calculating a mean square error of the signal. (See col. 11, lines 36-50)

But the reference Sunter fails to explicitly teach that wherein the signal has a high degree of correlation with an RF output of the RF circuit.

However, the reference of Sunter does teach a PLL having a loop filter connected at the output of the phase comparator whereby suggesting that wherein the signal has a high degree of correlation with an RF output of the RF circuit. (See figs. 5 & 9) One skilled in the art would know that, by definition, a loop filter filters out high frequency components that are not of interest, and passes only low frequency components that are of main interest to the PLL. (See pages 604-605 of "Digital Communications" by Bernard Sklar) Furthermore, applicant does teach in his specifications that "As long as the frequency components of interest are below the loop filter's cutoff frequency, the attenuation of frequency components above the cutoff frequency can actually improve the correlation between the observed signal and the RF output".

Therefore, it would have been obvious to one of ordinary skills in the art to incorporate this feature into the system of Sunter, in the manner as claimed, for the benefit of filtering out frequency components that are not of interest.

Re claim 27, Sunter further discloses that wherein the RF circuit is an all-digital frequency synthesizer. (See fig. 5)

Re claim 28, Sunter further discloses that wherein the RF circuit is an all-digital transmitter. (See fig. 5)

Re claim 29, Sunter further discloses that wherein the transmitter is used in a wireless communications network. (One skilled in the art would know that PLLs may operate in a Bluetooth environment.)

Re claim 30, Sunter further discloses that wherein the wireless communications network is Bluetooth compliant. (One skilled in the art would know that PLLs may operate in a Bluetooth environment.)

Re claim 31, Sunter further discloses that wherein the testing comprises a functional test or a compliance test of the RF circuit. (See fig. 5)

5. **Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sunter et al. (hereinafter Sunter) (US Patent 6,396,889 B1), as applied to claim 1 above, and further in view of Wong et al. (hereinafter Wong) (US Patent 5,295,079)**

Re claim 24, The method of claim 1, wherein the RF circuit contains an all- digital phase-locked loop (See fig. 5), and the method further comprises prior to the observing, setting the all-digital phase-locked loop to a certain bandwidth.

However, the reference of Wong does teach a loop configuration circuit which in response to the digital tester programs and via the LCP configures the loop type of the Device under test "DUT". (See col. 3, lines 19-26 & table 1)

Therefore, taking the combined teachings of Sunter & Wong as a whole, it would have been obvious to one of ordinary skills in the art to incorporate this feature into the

system of Sunter, as modified by Wong, in the manner as claimed, for the benefit of achieving synchronization.

6. **Claims (32-40) are rejected under 35 U.S.C. 103(a) as being unpatentable over Wong et al. (hereinafter Wong) (US Patent 5,295,079)**

Re claim 32, Wong discloses a circuit comprising: a processor coupled to a radio frequency (RF) circuit. (See fig. 2)

But the reference of Wong fails to explicitly teach that the processor containing circuitry to manipulate digital signals from the RF circuit to provide a performance metric for the RF circuit; and a control signal input coupled to the processor, wherein the control signal input can enable an observation and manipulation of the digital signals.

However, the reference of Wong does suggest that the teachings of digital tester (an intelligent digital controller) coupled to an input "keyboard" (See fig. 1: the input of element 4 & col. 1, lines 56-61), that performs tests, extract, and interpret data from the device under test (DUT). Furthermore, table 2 shows several of how to test some PLL dynamic performance parameters. (See fig. 2: 4 & col. 1, lines 45-48, 56-61, col. 2, lines 36-40, col. 4, lines 6-15)

Therefore, it would have been obvious to one of ordinary skills in the art to have incorporated this feature into the system of Wong, in the manner as claimed, for the benefit of testing some PLL dynamic performance parameters. (See col. 6, lines 29-31)

Re claim 33, the reference of Wong fails to disclose a latch coupled to the

processor, the latch to store the performance metric provided by the processor.

However, the reference of Wong does suggest the teaching of a digital tester, which may be a hand-held microprocessor-based controller with a keyboard and a multi-digit display that can be used for network servicing or for low-cost lab-quality engineering setups. (See col. 4, lines 13-16) Furthermore, one skilled in the art would know that latches may be used as storage elements, from which flip-flops are usually constructed. And registers, which are used extensively in the design of digital systems for storing data, consists of a set of flip-flops.

Therefore, it would have been obvious to one of ordinary skills in the art to have incorporated this feature into the system of Wong, in the manner as claimed, for the benefit of testing some PLL dynamic performance parameters. (See col. 6, lines 29-31)

Re claim 34, the reference of Wong further discloses that wherein the RF circuit is integrated onto a first integrated circuit, wherein the processor is integrated onto a second integrated circuit. (In Wong, see fig. 2)

Re claim 35, the reference of Wong fails to explicitly teach that wherein the first and the second integrated circuit are the same integrated circuit.

However, the reference of Wong does suggest the teaching of a IO controller integrated within the same integrated circuit as the RF circuit. (See fig. 2: 22 & 25)

Therefore, it would have been obvious to one of ordinary skills in the art to have incorporated this feature into the system of Wong, in the manner as claimed, for the

benefit of minimizing the time delay.

Re claim 36, the reference of Wong further discloses that wherein the RF circuit contains an all-digital phase-locked loop, and wherein the processor is coupled to an output of a phase detector. (In Wong, see fig. 2)

Re claim 37, the reference of Wong further discloses that wherein the RF circuit contains an all-digital phase-locked loop, and wherein the processor is coupled to a filtered output of a phase detector. (In Wong, see fig. 2: 24 & col. 3, lines 19-22, 50-56)

Re claim 38, the reference of Wong further discloses that wherein the RF circuit contains an all-digital phase-locked loop, and wherein the processor is coupled to an output of a phase detector and a filtered output of a phase detector. (In Wong, see fig. 2 & col. 3, lines 50-55)

Re claim 39, the reference of Wong further discloses that wherein the circuit permits the testing of the RF circuit in wafer, in packaged integrated circuit, in factory, and in field. (In Wong, see col. 1, lines 38-41, 48-51 & col. 4, lines 16-27)

Re claim 40, the reference of Wong further discloses that wherein the circuit permits the testing of the RF circuit, and wherein the testing is of a type selected from a group consisting of a phase trajectory error, a frequency lock, a frequency deviation, a

phase noise power, or combinations thereof. (In Wong, see fig. 2, 4b & 4c & col. 4, line 34 – col. 6, line 35 & table 2)

7. **Claims (41-44) are rejected under 35 U.S.C. 103(a) as being unpatentable over Staszewski et al (hereinafter Staszewski) (US Publication 2002/0191727 A1) in view of Sunter et al. (hereinafter Sunter) (US Patent 6,396,889 B1)**

Re claim 41, Staszewski discloses a circuit comprising: a reference phase accumulator coupled to a signal input, the reference phase accumulator containing circuitry to compute a reference phase (See fig. 4A: 62 & paragraph 44); a phase detector coupled to the reference phase accumulator, the phase detector containing circuitry to compute a difference between the reference phase and a variable phase (See fig. 4A: 68 & paragraph 44); a digitally-controlled oscillator (DCO) coupled to the phase detector (See fig. 4A: 74 & paragraph 44), a variable phase accumulator coupled to the DCO and the phase detector, the variable phase accumulator containing circuitry to compute the variable phase. (See fig. 4A: 66 & paragraph 46)

But the reference of Staszewski fails to teach that wherein the performance of the DCO can be ascertained by a test circuit outside of the circuit observing an output of the phase detector, wherein the test circuit manipulates the observed output and generates a performance metric for the DCO based, at least in part, on the manipulation.

However, Sunter does. (See figs. 5 & 11) Sunter suggests that wherein the performance of the DCO can be ascertained by a test circuit outside of the circuit

observing an output of the phase detector, wherein the test circuit manipulates the observed output and generates a performance metric for the DCO based, at least in part, on the manipulation.

Therefore, taking the combined teachings of Staszewski and Sunter as a whole, it would have been obvious to one of ordinary skills in the art to have incorporated this feature into the system of Staszewski, in the manner as claimed and as taught by Sunter, for the benefit of testing the performance of the PLL.

Re claim 42, the combination of Staszewski and Sunter further disclose a time-to-digital converter (TDC) coupled to the DCO and the phase detector, the TDC containing circuitry to compute a time difference between a reference clock and a variable clock. (In Staszewski, see fig. 6 & paragraph 51)

Re claim 43, the combination of Staszewski and Sunter further teach a loop filter coupled to the phase detector and the DCO (In Staszewski, see fig. 3A), the loop filter to provide a desired amount of attenuation to the computed difference between the reference phase and the variable phase. ("this is an inherent feature for loop filters within a PLL")

Re claim 44, Staszewski discloses a circuit comprising: a reference phase accumulator coupled to a signal input, the reference phase accumulator containing circuitry to compute a reference phase (See fig. 4A: 62 & paragraph 44); a phase

detector coupled to the reference phase accumulator, the phase detector containing circuitry to compute a difference between the reference phase and a variable phase (See fig. 4A: 68 & paragraph 44); a digitally-controlled oscillator (DCO) coupled to the phase detector (See fig. 4A: 74 & paragraph 44), a variable phase accumulator coupled to the DCO and the phase detector, the variable phase accumulator containing circuitry to compute the variable phase. (See fig. 4A: 66 & paragraph 46)

But the reference of Staszewski fails to teach a loop filter coupled to the phase detector and the DCO, the loop filter to provide a desired amount of attenuation to the computed difference between the reference phase and the variable phase, wherein the loop filter is of a type selected from a group consisting of a finite impulse response filter, an infinite impulse response filter or combination thereof.

However, in another embodiment (See fig. 3A), the reference of Staszewski does suggest a loop filter (40) coupled to the phase detector (38) and the DCO (42), the loop filter to provide a desired amount of attenuation to the computed difference between the reference phase and the variable phase ("this is an inherent feature for loop filters within a PLL"), wherein the loop filter is of a type selected from a group consisting of a finite impulse response filter, an infinite impulse response filter or combination thereof.("loop filters may be composed of any of these elements")

Therefore, it would have been obvious to one of ordinary skills in the art to incorporate these features into the system of Staszewski, in the manner as claimed, for the benefit of providing attenuation to frequency components above the cutoff frequency of the loop filter.

The reference of Staszewski discloses the limitations as claimed above, except he fails to teach that wherein the performance of the DCO can be ascertained by a test circuit outside of the circuit observing an output of the phase detector, wherein the test circuit manipulates the observed output and generates a performance metric for the DCO based, at least in part, on the manipulation.

However, Sunter does. (See figs. 5 & 11) Sunter suggests that wherein the performance of the DCO can be ascertained by a test circuit outside of the circuit observing an output of the phase detector, wherein the test circuit manipulates the observed output and generates a performance metric for the DCO based, at least in part, on the manipulation.

Therefore, taking the combined teachings of Staszewski and Sunter as a whole, it would have been obvious to one of ordinary skills in the art to have incorporated this feature into the system of Staszewski, in the manner as claimed and as taught by Sunter, for the benefit of testing the performance of the PLL.

8. **Claims (48-50, 52-54) are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al (hereinafter Kim) (US Patent 6,885,700 B1) in view of Ortiz Perez et al. (hereinafter Perez) (US Patent 5,966,428)**

9. Re claim 48, Kim discloses a method for operating a cellular phone, comprising: performing built-in self-test (BIST) on a parameter associated with the cellular phone. (See col. 6, lines 9-49 "PLL")

But the reference of Kim fails to teach reporting to a cellular service provider

through a wireless medium when the BIST reports the parameter to be degraded beyond a limit.

However, Perez does. (See abstract & col. 5, line 26 – col. 6, line 15) Perez discloses a self-diagnostic system for checking all functions of a cellular-transceiver, and reporting the results to an off-site monitoring center by means of the cellular network.

Therefore, taking the combined teachings of Kim and Perez as a whole, it would have been obvious to one of ordinary skills in the art to incorporate this feature into the system of Kim, in the manner as claimed and as taught by Perez, for the benefit of reporting the results to an off-site monitoring center.

Re claim 49, the combination of Kim and Perez fails to explicitly teach that wherein the performing step is done on power-up of the cellular phone.

However, the reference of Perez does teach that the system for checking all the functions of the cellular is a self-diagnostic system. (See abstract) Furthermore, it also teaches that it is an auto-diagnostic system. One skilled in the art would know that auto-diagnostic system operate at power-up of the cellular phone to assure that the tranceiver is working properly.

Therefore, it would have been obvious to one of ordinary skills in the art to incorporate this feature into the system of Kim, as modified by Perez, in the manner as claimed, for the benefit of checking if the cellular phone is working properly.

Re claim 50, the combination of Kim and Perez further discloses that wherein the parameter is an RF system parameter. (In Kim, see col. 6, lines 9-49 "PLL")

Re claim 52, the combination of Kim and Perez fails to explicitly teach that a step of notifying a user of the cellular phone that the parameter is degraded beyond a limit.

However, the reference of Perez does teach a self-diagnostic system for checking all functions of a cellular-transceiver, and reporting the results to an off-site monitoring center by means of the cellular network in order to check if the tranceiver is working properly.

Therefore, it would have been obvious to one of ordinary skills in the art to incorporate this feature into the system of Kim, as modified by Perez, in the manner as claimed, for the benefit of checking if the cellular phone is working properly.

Re claim 53, the combination of Kim and Perez further discloses that wherein the notifying step is done wirelessly. (In Perez, see abstract "cellular network")

Re claim 54, the combination of Kim and Perez fails to explicitly teach that wherein the notifying step is done through a service bill.

However, the reference of Perez does teach notifying the results to an off-site monitoring center by means of the cellular network. One skilled in the art would know that service bill can also be broadcast wirelessly.

Therefore, it would have been obvious to one of ordinary skills in the art to

incorporate this feature into the system of Kim, as modified by Perez, in the manner as claimed, for the benefit of optimizing the communication system.

10. **Claim 51 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al (hereinafter Kim) (US Patent 6,885,700 B1) and Ortiz Perez et al. (hereinafter Perez) (US Patent 5,966,428), as applied to claim 48 above, and further in view of Reddy et al. (hereinafter Reddy) (US Patent 6,636,979 B1)**

11. Re claim 51, the combination of Kim and Perez fails to explicitly teach that wherein the RF system parameter is a distortion in a phase error trajectory.

However, Reddy does. (See col. 5, lines 58-65) Reddy discloses a phase error measurement circuit used to measure the phase error between two clocks. The circuit can be used as part of a built-in self test (BIST) function to estimate phase error in a PLL.

Therefore, taking the combined teachings of Kim, Perez, and Reddy as a whole, it would have been obvious to one of ordinary skills in the art to incorporate this feature into the system of Kim, as modified by Perez, in the manner as claimed and as taught by Reddy, for the benefit of detecting the phase error.

12. **Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wong et al. (hereinafter Wong) (US Patent 5,295,079)**

Re claim 1, Wong discloses a method for testing a radio frequency (RF) circuit comprising: observing a signal from the RF circuit (See fig. 2: 4, 26 & col. 1, lines 42-60

& col. 3, lines 50-55), wherein the signal is a digital signal from within a processing portion of the RF circuit (See fig. 2), and wherein the observing occurs outside of the RF circuit (See fig. 2: 4, 26 & col. 1, lines 42-60); manipulating the signal outside of the RF circuit (See fig. 2: 4, 26 & col. 1, lines 42-60); and producing a metric for the test outside of the RF circuit based on results from the manipulating. (See fig. 2: 4, 26 & col. 1, lines 42-60)

But the reference of Wong fails to explicitly teach that wherein the signal has a high degree of correlation with an RF output of the RF circuit.

However, the reference of Wong does teach a PLL having a loop filter connected at the output of the phase comparator whereby suggesting that wherein the signal has a high degree of correlation with an RF output of the RF circuit. (See figs. 5 & 9) One skilled in the art would know that, by definition, a loop filter filters out high frequency components that are not of interest, and passes only low frequency components that are of main interest to the PLL. (See pages 604-605 of "Digital Communications" by Bernard Sklar) Furthermore, applicant does teach in his specifications that "As long as the frequency components of interest are below the loop filter's cutoff frequency, the attenuation of frequency components above the cutoff frequency can actually improve the correlation between the observed signal and the RF output".

Therefore, it would have been obvious to one of ordinary skills in the art to incorporate this feature into the system of Wong, in the manner as claimed, for the benefit of filtering out frequency components that are not of interest.

Allowable Subject Matter

13. Claims (12, 18, 26, 45-47) are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- Bui et al (US Patent 5,126,690) disclose a test circuit at the output of the phase detector.
- Ghaderi et al (US Patent 5,870,002) disclose a test circuit at the output of the phase detector.

Contact

Any inquiry concerning this communication or earlier communications from the examiner should be directed to LEON FLORES whose telephone number is (571)270-1201. The examiner can normally be reached on Mon-Fri 7-5pm Alternate Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad Ghayour can be reached on 571-272-3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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/L. F./
Examiner, Art Unit 2611
September 5, 2009

/David C. Payne/

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